REMARKS

Claims 1-18, 22, and 23 are pending in the present application. No claims were canceled; claims 2, 8, and 18 were amended; and no claims were added. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

I. 35 U.S.C. §102, Anticipation, Claims 1, 7, and 10

The Examiner has rejected claims 1, 7, and 10 under 35 U.S.C. Section 102 as being anticipated by *Kelley et al* (U.S. Patent No. 5,517,603). This rejection is respectfully traversed.

With regard to claim 1, the Examiner states:

> As per claim 1, Kelley et al discloses an apparatus for optimizing processing of graphics data (abstract), the apparatus comprising: a plurality of logic units (fig 7), wherein the plurality of logic units are used to perform a graphics operation (fig 7) in which a set of constants is required for the graphics operation (column 13 lines 1-15 and column 15 lines 38-52, Z-value could be a constant value); a first set of connections connecting the plurality of logic units to each other (fig 7), wherein the first set of connections are used to configure the plurality of logic units (column 13 lines 1- 15 and column 15 lines 38-52; fig 7, stage 2 is one logic circuit and stage 3 in another logic circuit) to calculate the set of constants (column 15 lines 38-52, the pixel interpolation token is received from one connection and the Z-value is calculated for stage 2 and the alpha value is calculated for stage 30; and a second set of connections connecting the plurality of logic units (fig 7), wherein the second set of connections configure the plurality of logic units to perform the graphics operation (column 13 lines 1-15 and column 15 lines 38-52) in which the graphics operation uses the constants calculated through the first set of connections (fig 7 and column 13 lines 1-15 and columns 25 lines 60-65, control tokens from a connection configure the chip (logic unit) to perform its particular function, like using the Z-value (constant) to generate another result.

(*Office Action*, dated October 7, 2004, pages 2-3). Independent claim 1, which is representative of independent claim 10 with regard to similarly recited subject matter, reads as follows:

1. An apparatus for optimizing processing of graphics data, the apparatus comprising:

a plurality of logic units, wherein the plurality of logic units are used to perform a graphics operation in which a set of constants is required for the graphics operation;

a first set of connections connecting the plurality of logic units to each other, wherein the first set of connections are used to configure the plurality of logic units to calculate the set of constants; and

a second set of connections connecting the plurality of logic units, wherein the second set of connections configure the plurality of logic units to perform the graphics operation in which the graphics operation using the constants is calculated through the first set of connections.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir.1990). The *Kelley* reference cited by the Examiner does not anticipate the present invention as recited in claim 1, because *Kelley* fails to teach each and every element of the claim.

The rejected independent claim 1 includes a plurality of logic units, wherein the plurality of logic units are used to perform a graphics operation in which a set of constants is required for the graphics operation, a first set of connections connecting the plurality of logic units to each other, wherein the first set of connections are used to configure the plurality of logic units to calculate the set of constants; and a second set of connections connecting the plurality of logic units, wherein the second set of connections configure the plurality of logic units to perform the graphics operation in which the graphics operation using the constants is calculated through the first set of connections. The feature of using a set of connections to configure a plurality of logic units to calculate a set of constants, and then using the set of constants to perform a graphics operation is not taught by *Kelley*.

As discussed in the Abstract, *Kelley* is directed towards a rendering device for providing 3-D graphics rendering in a computer system. *Kelley* utilizes a hardware scanline rendering approach to minimize the bandwidth requirements between a system frame buffer and the rendering device. The minimization of bandwidth requirement allows for the rendering device to be used with existing computer system designs while

keeping design changes at a minimum. Using the *Kelley* system, for a given desired performance of a combined computer system and rendering device, the cost of both the computer system without the rendering device, and the cost of the rendering device itself may be reduced. The rendering device is generally comprised of a bus attachment for coupling to the system bus of the computer system and a scanline rendering device and a scanout device for transferring the scanline of shaded pixel values to the system frame buffer. In summary, the *Kelley* invention is a device for transferring shaded pixel values to the system frame buffer.

In the following cited passages, the Examiner alleges that *Kelley* teaches an apparatus for optimizing processing of graphics data by using a set of connections to configure a plurality of logic units to calculate a set of constants, and then using the set of constants to perform a graphics operation:

> Data and control information is transferred between various stages in the rendering pipeline area as "tokens". "Tokens" as utilized in the preferred embodiment, refer to a fixed structure for sending and receiving data and control information. In any event, prior to receiving object, the rendering pipeline must be provided with setup information to define the rendering functions that will be performed. In the preferred embodiment, this occurs by propagation of a global setup token through the pipeline. The global mode setup token is described in greater detail in the section entitled Tokens. Briefly, the global mode setup token is generated by the control processor (i.e., FIG. 6a or the host processor per FIG. 6b) and is used to enable diffuse or specular shading, shadowing and a transparency mode.

(*Kelley*, column 13, lines 1-15)

> Stage 2 processing begins when a Pixel Interpolation token is received, Step 823. First a corresponding Z-value for the pixel is calculated, step 824. The Z value for the pixel is calculated by directly evaluating a linear interpolation (LIRP) function, using an interpolation weight value contained within the pixel interpolation token. When comparing Z-values, a lower Z-value means that the object is closer to the viewer. In this context, this means that a first object with a higher Z-value than a second object will be behind and thus hidden by the second object. It should be noted that the Z-buffer will always be initiated to a maximum Z-value so that it will have a valid value to compare incoming Z-values with. This horizontal interpolation of the Z-values of various pixels in the span is described in more detail below.

(*Kelley*, column 15, lines 38-52)

> Unlike general tokens and set-up tokens, control tokens are generated by the control processor (with one exception being the Scanout Data token, which is also generated by the Z chip 705 when scanning out its buffer). Control tokens are commands to target chips in the pipeline to perform a particular function, e.g., swap buffers, output scanline, etc. It is through the use of control tokens that operation and resources of the pipeline are managed.

(*Kelley*, column 25, lines 58-65)

In the first cited passage above, *Kelley* teaches that tokens are fixed structures for sending and receiving setup data and control information between various stages in the rendering pipeline area, defining the rendering functions that will be performed. In the column 15 section, *Kelley* teaches that liner interpolation is used for calculation of a Z-value for each pixel for the purpose of comparing Z-values in order to determine which objects are closer to the viewer. In the column 25 section, *Kelley* teaches control tokens as commands to target chips in the pipeline to perform particular functions in order to mange the operations and resources of the pipeline.

These sections in *Kelley* that the Examiner referenced do not teach an apparatus for optimizing processing of graphics data by using a set of connections to configure a plurality of logic units to calculate a set of constants, and then using the set of constants to perform a graphics operation as recited in claim 1 of the present invention. Rather, to the contrary, the column 13 section teaches the use of data tokens that are not constants, but used to enable diffuse or specular shading, shadowing and a transparency mode. *Kelley's* column 15 section teaches the linear interpolation of a Z-value for each pixel, the Z-value of each pixel differing and not remaining constant, with Z-values being compared to determine that a first object with a higher Z-value will be behind a second object with a lower Z-value, and thus hidden by the second object. The column 25 section of *Kelley* teaches control tokens that are commands used to manage the pipeline, not constant values. Neither the column 13 section, the column 15 section, nor the column 25 section of *Kelley* teach a set of connections that are used to configure a plurality of logic units to either calculate a set of constants or to perform graphics operations using the set of constants. Furthermore, because a rendering pipeline, as

shown below in Figure 7 of *Kelley*, is neither a set of connections nor a plurality of logic units, the cited sections in *Kelley* do not even teach sets of connections or a plurality of logic units.

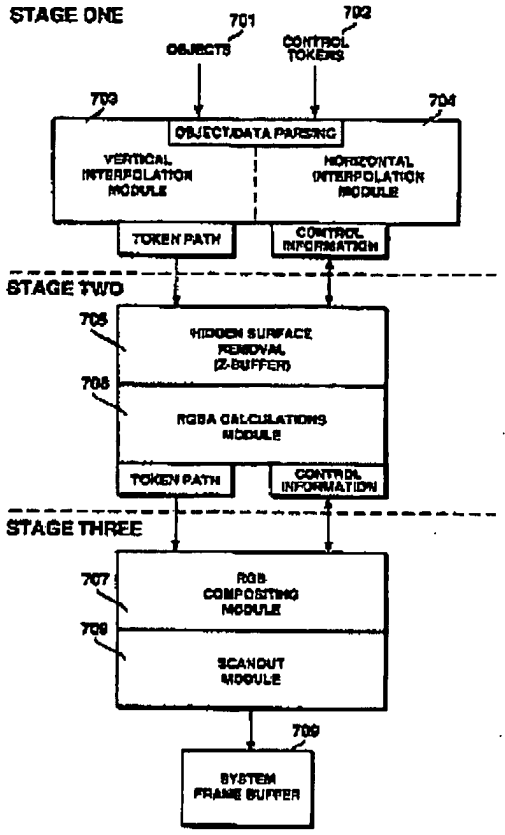

FIGURE 7

In addition, in the rejection of independent claim 1, the Examiner further states that the Z-value in *Kelley* "could be a constant value." The Z-value in *Kelley* is the third coordinate of a 3-D graphical object, which is a depth coordinate (*Kelley*, column 2, lines 43-46). *Kelley* teaches determining a Z-value for a pixel from Z-values of endpoints of a horizontal span (*Id.*, claim 9). Rather than teaching that the Z-value is a constant, *Kelley* teaches that the Z-value is a value based on a 3rd dimension ordinate for a pixel, which is determined from a range of Z-values for each pixel. In *Kelley*, an initial Z-value is used as a reference point, not as a constant, in determining that a first object with a

higher Z-value than a second object will be behind and thus hidden by the second object (*Id.*, column 15 lines 45-47). *Kelley* also teaches a method for shading, in that the Z-values are read from a buffer and compared with shadow projections for each light source (*Id.*, column 21 lines 59-61). In *Kelley*, each and every pixel that represents the objects depicted in the graphics, whether hidden or shaded, has its own Z-value, thus emphasizing the variable nature of the Z-values.

As the Z-values in *Kelley* must be of a variable nature for the purpose of comparing the differing Z-values for each pixel, it is not only apparent that the Z-values are not constants, but also evident that these Z-values cannot be constants. Because each pixel may be depicted as hidden or in view, shaded or un-shaded, based on its corresponding Z-value, a unique Z-value must be calculated for each pixel every time the graphics are rendered. While Z-values are useful as references for comparisons, Z-values that were held constant would be detrimental to *Kelley*'s graphics rendering. Moreover, *Kelley* never even mentions sets of connections or logic units. In contrast, the present invention, as recited in independent claims 1 and 10, is an apparatus for optimizing processing of graphics data by using a set of connections to configure a plurality of logic units to calculate a set of constants, and then using the set of constants to perform a graphics operation. Therefore, *Kelley* fails to teach all elements of the claimed invention, and thus fails to anticipate the invention as recited in independent claims 1 and 10.

Furthermore, *Kelley* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Kelley* actually teaches away from the presently claimed invention because it never mentions sets of connections or logic units, and it teaches the use of variable Z-values for hiding or shading displayed objects, not an apparatus for optimizing processing of graphics data by using a set of connections to configure a plurality of logic units to calculate a set of constants, and then using the set of constants to perform a graphics operation. Absent the Examiner pointing out some teaching or incentive to implement *Kelley* using sets of connections to configure logic units to calculate a set of constants and use the set of constants for optimized processing of graphics data, one of ordinary skill in the art would not be led to modify *Kelley* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Kelley* in this manner, the

presently claimed invention can be reached only through an improper use of hindsight using the Applicant's disclosure as a template to make the necessary changes to reach the invention.

Therefore, the rejection of independent claims 1 and 10 under 35 U.S.C. §102 has been overcome.

Claims 3-7, and 11-17 are dependent claims depending on independent claims 1 and 10, respectively. Applicant has already demonstrated claims 1 and 10 to be in condition for allowance. Applicant respectfully submits that claims 3-7, and 11-17 are also allowable, at least by virtue of their dependency on allowable claims.

Thus, the rejection of claims 1, 7, and 10 under 35 U.S.C. §102 has been overcome.

II. **35 U.S.C. §103, Obviousness, Claims 3 and 13**

The Examiner has rejected claims 3 and 13 under 35 U.S.C. §103(a) as being unpatentable over *Kelley et al* (U.S. Patent No. 5,517,603) in view of *Rohner* (U.S. Patent No. 6,064,392). This rejection is respectfully traversed.

The Examiner bears the burden of establishing a prima facie case of obviousness based on prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). For an invention to be prima facie obvious, the prior art must teach or suggest all claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

The combination of *Kelley* and *Rohner* fail to teach or suggest the present invention as cited in claims 3 and 13. Although *Rohner* may teach a graphics operation that is a generation of a fog factor (*Rohner*, Abstract), the *Kelley* reference still does not teach or suggest all the claim limitations in claim 3 (dependent upon claim 1) and in claim 13 (dependent upon claim 10), as argued in response to the rejections of claims 1 and 10 above. Claims 3 and 13 are patentable over the cited references because the combination of the *Rohner* reference with *Kelley* would not teach the presently claimed invention. The features relied upon as being taught in *Kelley*, the set of connections to configure the plurality of logic units to calculate and use constants in the optimized processing of graphics data operations, are not taught or suggested by that reference, as

explained above. As a result, a combination of these references would not reach the claimed invention in claims 3 and 13.

Thus, the rejection of claims 3 and 13 under § 103 in view of *Kelley* has been overcome.

III. 35 U.S.C. §103, Obviousness, Claims 4 and 14

The Examiner has rejected claims 4 and 14 under 35 U.S.C. §103(a) as being unpatentable over *Kelley et al* (U.S. Patent No. 5,517,603) in view of *Harris* et al. (U.S. Patent No. 6,304, 265). This rejection is respectfully traversed.

The combination of *Kelley* and *Harris* fail to teach or suggest the present invention as cited in claims 4 and 14. Although *Harris* may teach a graphics operation that is a viewport transformation (*Harris*, column 7 lines 48-56), the *Kelley* reference still does not teach or suggest all the claim limitations in claim 4 (dependent upon claim 1) and in claim 14 (dependent upon claim 10), as argued in response to the rejections of claims 1 and 10 above. Claims 4 and 14 are patentable over the cited references because the combination of the *Harris* reference with *Kelley* would not teach the presently claimed invention. The features relied upon as being taught in *Kelley*, the set of connections to configure the plurality of logic units to calculate and use constants in the optimized processing of graphics data operations, are not taught or suggested by that reference, as explained above. As a result, a combination of these references would not reach the claimed invention in claims 4 and 14.

Thus, the rejection of claims 4 and 14 under § 103 in view of *Kelley* has been overcome.

IV. 35 U.S.C. §103, Obviousness, Claims 5-6, 9, and 11-12

The Examiner has rejected claims 5-6, 7, 9, and 11-12 under 35 U.S.C. § 103(a) as being unpatentable over *Kelley* et al (U.S. Patent No. 5,517,603) in view of *Gholizadeh* et al. (U.S. Patent No. 5,369, 737). This rejection is respectfully traversed.

The combination of *Kelley* and *Gholizadeh* fail to teach or suggest the present invention as cited in claims 5, 6, 9, 11, and 12. The *Kelley* reference still does not teach or suggest all the claim limitations of claims 5, 6, 9, 11, and 12, as argued in response to

the rejections of claims 1 and 10 above. Claims 5, 6, 9, 11, and 12 are patentable over the cited references because the combination of the *Gholizadeh* reference with *Kelley* would not teach the presently claimed invention. The features relied upon as being taught in *Kelley*, the set of connections to configure the plurality of logic units to calculate and use constants in the optimized processing of graphics data operations, are not taught or suggested by that reference, as explained above. As a result, a combination of these references would not reach the claimed invention in claims 5, 6, 9, 11, and 12.

Thus, Applicant respectfully requests withdrawal of the rejection of claims 5-6, 9, and 11-12 under 35 U.S.C. §103.

V. 35 U.S.C. §103, Obviousness, Claims 15-17

The Examiner has rejected claims 15-17 under 35 U.S.C. § 103(a) as being unpatentable over *Kelley et al* (U.S. Patent No. 5,517,603). This rejection is respectfully traversed. Claims 15 -17 are dependent claims depending on independent claim 10. As shown above, *Kelley* still does not teach or suggest all of the claim limitations in claim 10, from which claims 15-17 depend. The features relied upon as being taught in *Kelley*, the set of connections to configure the plurality of logic units to calculate and use constants in the optimized processing of graphics data operations, are not taught or suggested by that reference, as explained above.

Thus, the rejection of claims 15-17 under § 103 in view of *Kelley* has been overcome.

VI. 35 U.S.C. §103, Obviousness, Claims 22 and 23

The Examiner has rejected claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over *Cobb* et al. (U.S. Patent No. 6,603,474) in view of *Kelley et al* (U.S. Patent No. 5,517,603). This rejection is respectfully traversed.

The combination of *Kelley* and *Cobb* fail to teach or suggest the present invention as cited in claims 22 and 23. Although *Cobb* may teach a geometry engine connected to the raster engine that rasterizes the processed graphics data for display (*Cobb*, column 4 lines 32-38), the *Kelley* reference still does not teach or suggest all the claim limitations in claims 22 and 23, as argued in response to the rejections of claims 1 and 10 above.

Claims 22 and 23 are patentable over the cited references because the combination of the *Cobb* reference with *Kelley* would not teach the presently claimed invention. The features relied upon as being taught in *Kelley*, the set of connections to configure the plurality of logic units to calculate and use constants in the optimized processing of graphics data operations, are not taught or suggested by that reference, as explained above. As a result, a combination of these references would not reach the claimed invention in claims 22 and 23.

Thus, the rejection of claims 22 and 23 under § 103 in view of *Kelley* has been overcome.

VII. Objection to Claims, Claims 2, 8, and 18

The Examiner has stated that claims 2, 8, and 18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, the claims have been rewritten to overcome this objection.

VIII. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 12/17/04

Respectfully submitted,

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